

### **REMARKS**

Claims 7-15 are pending. Claims 7, 10, and 11 have been amended. Claims 12-15 are newly presented. Claims 1-6 have been cancelled. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

#### ***Claim Objections***

Claims 10 and 11 were objected to for containing a typographical error. Applicant has amended the claims to correct these errors in accordance with the Examiner's suggestions. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this objection.

#### ***Claim Rejections Under 35 U.S.C. § 103***

Claims 7-11 were rejected under 35 U.S.C. § 103(a) over Applicants Admitted Prior Art (AAPA) in view of Rostoker et al. (U.S. Patent No. 6,181,011). Applicant respectfully traverses this rejection.

Amended claim 1 recites, in part, a method for fabricating a semiconductor memory device that includes forming a plurality of line patterns, each being formed by stacking a conductive layer, an insulating hard mask, and a spacer allocated at sidewalls of each of the line patterns, removing the entire insulating hard mask and the entire spacer formed in the peripheral circuit region, and forming a conductive spacer at sidewalls of each line pattern in the peripheral circuit region.

In contrast, AAPA discloses a spacer 12 at the sidewalls of line pattern 103B in the peripheral circuit region 102 that is not removed. AAPA is also silent regarding the claimed conductive spacer of the presented invention. The spacer 12 in the peripheral circuit region 102 is not conductive (See, for example, page 2, lines 5-15 and page 7, lines 6-9). As illustrated in, for example, Figure 4B, the spacer 45 in a peripheral circuit region 42 is removed, and then, a new conductive spacer 48 is formed at the sidewalls of the line patterns 46B. Additionally, in AAPA a hard mask 11 formed on a conductive layer 10 of the line pattern 103B in the peripheral circuit region 102 is not removed until a deep contact hole 19 is formed, and even then, the mask 11 is only partially removed (See, for example, Figure 3). Accordingly, AAPA fails to teach or suggest at least a conductive spacer that is formed after the initial spacer is removed and the complete removal of the hard mask. Rostoker does not remedy at least the deficiencies of AAPA discussed above since Rostoker merely discloses a method for controlling critical dimensions in integrated circuits. Accordingly, no

combination of AAPA and Rostoker teach or suggest a method for fabricating a semiconductor memory device that includes forming a plurality of line patterns, each being formed by stacking a conductive layer, an insulating hard mask, and a spacer allocated at sidewalls of each of the line patterns, removing the entire insulating hard mask and the entire spacer formed in the peripheral circuit region, and forming a conductive spacer at sidewalls of each line pattern in the peripheral circuit region, as recited in amended claim 1.

Claims 8-11 are believed allowable for at least the reasons presented above with respect to claim 7 by virtue of their dependence upon claim 7. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

### ***New Claims***

Claims 12-15 are newly presented, fully supported by the originally filed specification and believed allowable over the prior art of record for at least the reasons presented above with respect to claim 7 by virtue of their dependence upon claim 7.

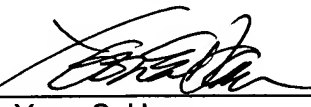
### ***Conclusion***

Therefore, all objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Should any issues remain unresolved, the Examiner is encouraged to contact the undersigned attorney for Applicants at the telephone number indicated below in order to expeditiously resolve any remaining issues.

Respectfully submitted,

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Date: July 21, 2005